ECR #: 31
Title: Relationship between xRDY# and AD_STBx
Release Date: May 12, 1997
Impact: Clarification
Spec Version: A.G.P. 1.0

Summary: This ECR clarifies when data actually transfers with respect to xRDY# when using 2x protocol.

Background: There has been some confusion on 2x data transfers. The 2x diagrams of chapter 3 use worst case timings whereas Figure 4-6 uses typical timing values. If this difference is not understood, there appears to be some disagreement between the protocol diagrams in chapter 3 and the Figure 4-6 in the electrical section.

Change Current Specification as shown:

Add the following to a new section in chapter 3.

Relationship between xRDY# and AD_STBx

All 2x diagrams in chapter 3 and Appendix B are drawn from the worse case timings from the view point of the receiver. Therefore it appears that data is transferred the clock after **xRDY#** is asserted, when per section 4.1.3. the data can actually occur the clock in which **xRDY#** is asserted.
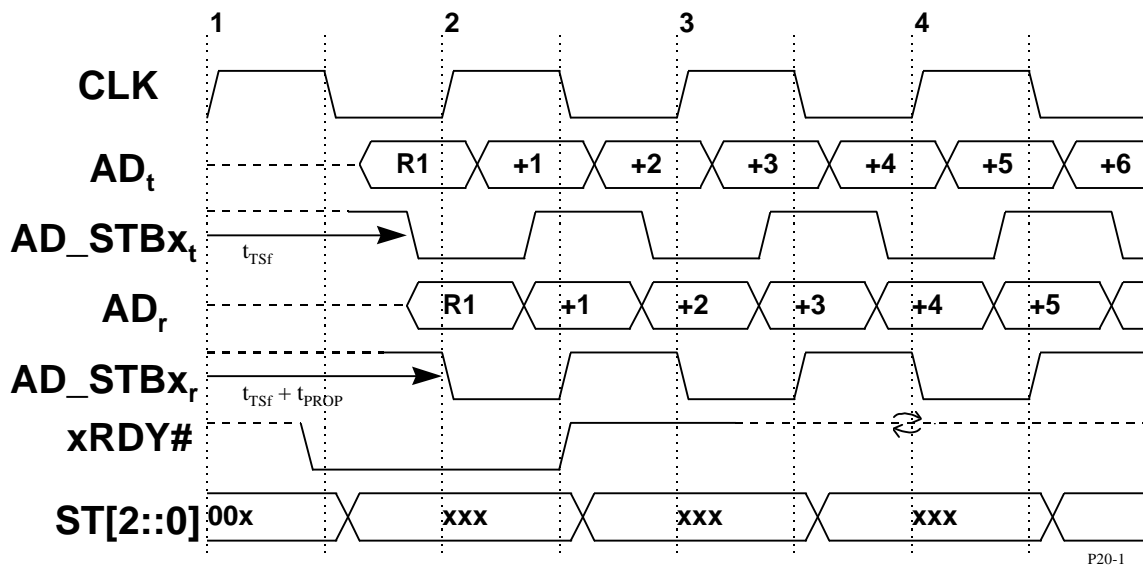
P20-1

In figure P20-1, the signal names that have a subscript t, indicate the signal at the transmitter of the data, while the subscript r indicates the signal at the receiver. **AD_STBx$_t$** is the strobe driven by the transmitter and is required to be valid within t_{TSf} which is 2-12 ns[1] after the rising edge of **CLK**. **AD_STBx$_r$** is the strobe as seen by the receiving agent. It is delayed t_{PROP} from the transmitter's delay by

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[1] See table 4-4

up to an additional 3 ns[2]. The maximum total of these delays puts the falling edge of **AD_STBx$_r$** on the rising edge of clock 2. This makes it appear as though data R1 is driven off of clock 2 with no propagation delay, while in fact it was driven from clock 1 with nearly a full clock of delay. Section 4.1.3. discusses 2x transactions, when data is valid and when it may be used.

Figure 4-6 clearly shows that the first data transfers during T1 and illustrates a more typical value where t$_{TSf}$ and t$_{PROP}$ are not at the maximum delays allowed. When the agent providing the data using the minimum times, both the falling and rising edges of **AD_STBx** can occur during T1 or clock 1 in the figure. The agent that receives the data is required to handle the data transferring anywhere between the minimum to the maximum delays of the transmitting agent and the motherboard.

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[2] See table 4-8